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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,797	03/03/2004	Yohei Akita	520.43578X00	4357

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EXAMINER	
CODY, DILLON J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,797	AKITA, YOHEI	
	Examiner	Art Unit	
	Dillon J. Cody	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3 March 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 are pending.

Papers Filed

2. Examiner acknowledges receipt of claims, disclosure, drawings, and information disclosure statement, all filed 3 March 2004 and declaration filed 22 July 2004.

Priority

3. Applicant's claim for foreign priority date 6 May 2003 is hereby acknowledged.

Title

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Specification

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

6. Claims 10-11 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim 10. See MPEP § 608.01(n). Accordingly, the claims have not been further treated on the merits.

7. Claims are objected to because of the following informalities:

a. Claim 3, line 4: "the corresponding one..." should read "a corresponding one..." as a corresponding instruction has not yet been introduced.

b. Claim 6, line 5: the phrasing of this sentence makes it unclear whether the instruction, ALU or control circuit "compris[es] an instruction defining..." For purposes of examination, the claim will be interpreted as the instruction comprising the further limitations.

c. Claim 6, lines 5-8: For the instruction to comprise both "an instruction defining..." **AND** "instructions defining..." is redundant. The first limitation (a single instruction) is a subset of the second limitation (multiple instructions). The claim will be interpreted as the two limitations being in the alternative (a single instruction **OR** a plurality of instructions).

d. Claim 7, line 4: Lines 1-2 require either a "plurality of instructions" or "instruction blocks" to be defined. Lines 3-4 require "execution order dependency between said instruction blocks". Examiner asserts that in the case where a "plurality of instructions" is defined and "instruction blocks" are not, lines 3-4 do not make sense. Examiner will interpret the claim to read "...and an execution

order dependency between said instruction blocks is described, when said instruction blocks are defined" for purposes of examination.

e. Claim 8, lines 4, 6 and 8: As this claim is dependent on claim 7, which gives the option for "instruction blocks" to be defined by the program or not, this reference to "instruction blocks" is improper. Examiner will interpret the claim to read "...said instructions blocks, if they have been defined" for each appearance of the term for purposes of examination.

8. Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claim 5 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Line 13 recites "said corresponding ALU is executable". Examiner does not see how an ALU can be executed.

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 2-4 and 8 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

13. Claim 2 recites the limitation "the executable one of said plurality of instructions" in line 4. There is insufficient antecedent basis for this limitation in the claim. Examiner recommends amending "the" to "an".

14. Claim 4 recites "the executable ones of said plurality of instructions" in line 3. Examiner recommends either changing "ones" to "one" in claim 4, or amending claim 2 to include the possibility of multiple executable instructions.

15. Claim 8 recites the limitation "instruction blocks" in lines 4, 7 and 9. There is insufficient antecedent basis for this limitation in the claim. The claim is dependent on either claim 6 or claim 7, and claim 6 has not introduced the term "instruction blocks".

16. Claim 3 is rejected on the basis of its dependency.

Claim Rejections - 35 USC § 101

17. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 6-11 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. A "program" doe not constitute tangible subject matter and is, hence, non-statutory.

Claim Rejections - 35 USC § 102

18. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

19. Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Mohamed et al. (U.S. Patent No. 6,415,376) hereinafter referred to as Mohamed.

20. As per claim 1, Mohamed teaches a logic circuit comprising an arithmetic logic unit (ALU) performing a logical operation or an arithmetical operation, and a control circuit controlling said ALU, wherein said control circuit receives, as an input, a program including a plurality of instructions defining the type of an operation to be executed on an ALU and information showing a dependency between said plurality of instructions and controls said ALU according to said program. *As disclosed in col. 1-2, Mohamed teaches using a decoder/issue logic to break a long instruction word into multiple issue groups, taking into account data dependencies of the instructions. The information dictating which instructions belong to which issue group is included in the instruction word. The examiner asserts that the instructions inherently define which operation to perform by means of their opcodes. If they did not contain such information, the instruction would be useless.*

21. As per claim 2, Mohamed teaches the logic circuit according to claim 1, wherein said control circuit decides an execution order of said plurality of instructions according to said information showing a dependency to supply the executable one of said plurality of instructions to said ALU. (Col. 1 lines 37-50)

22. As per claim 3, Mohamed teaches the logic circuit according to claim 2, wherein said information showing a dependency is information on an antecedent instruction which must have been executed in order to execute the corresponding one of said plurality of instructions, said control circuit decides whether said antecedent instruction is executed. (Col. 1 lines 37-50)

23. As per claim 4, Mohamed teaches the logic circuit according to claim 2, wherein said logic circuit has a plurality of said ALUs, said control circuit outputs the executable ones of said plurality of instructions to said ALUs in parallel. (Col. 1 lines 31-35)

24. As per claim 5, Mohamed teaches the logic circuit according to claim 1, wherein said logic circuit is a re-configurable processor, *The examiner asserts that the processor is reconfigured by the opcode of each instruction to perform the corresponding operation associated therewith.*

said ALUs include a plurality types of operations and are arrayed, (Col. 1 lines 19-30) *The examiner asserts that any plurality of ALUs constitutes an array, no matter how many rows or columns they form.*

said program includes definition of data used as an input and output,of an operation, specification of said operation type to said ALU, specification of a connection state of wiring between said arrayed ALUs, and information on input data necessary for the corresponding one of said arrayed ALUs to perform an operation, *The examiner asserts that instructions inherently contain operand data dictating which data to perform the operation on and where to put the result. The opcode is inherent, as an instruction which does not specify an operation is useless. The opcode and operands further specify a wiring state as they control the processor to make the proper connections between the register file (or other data source) and the functional unit. The operands further constitute "information on input data" as they dictate which data to use as input for the operation.*

said control circuit controls the connection state of wiring between said arrayed ALUs according to said inputted program to decide whether said corresponding ALU is executable. (Col. 1 lines 37-55)

25. As per claim 6, Mohamed teaches a program which allows a logic circuit having an ALU performing a logical operation or an arithmetical operation and a control circuit controlling the ALU to execute a desired operation by giving an instruction to said ALU via said control circuit, comprising an instruction defining the type of an operation to be

executed on said ALU and instructions defining the types of operations to be executed on a plurality of ALUs, wherein an execution order dependency existing in said instruction or between said instructions is described. *As disclosed in col. 1-2, Mohamed teaches using a decoder/issue logic to break a long instruction word into multiple issue groups, taking into account data dependencies of the instructions. The information dictating which instructions belong to which issue group is included in the instruction word. The examiner asserts that the instructions inherently define which operation to perform by means of their opcodes. If they did not contain such information, the instruction would be useless.*

26. As per claim 7, Mohamed teaches the program according to claim 6, wherein said plurality of instructions or instruction blocks having said instructions are defined, and an execution order dependency between said instruction blocks is described. (Col. 1 lines 20-55)

27. As per claim 8, Mohamed teaches the program according to claim 6 or 7, which describes:

an execution order dependency existing in said instruction or between said instructions or said instruction blocks; (Col. 1 lines 20-55)

operations having said instruction, said instructions or said instruction blocks; *The examiner asserts that opcodes are inherent in an instruction as an operation which does not define a function is useless.*

data of an input or output of said instruction, said instructions, or said instruction blocks; *Operands are inherent in an instruction, as data inputs and outputs must be defined for an operation to perform on the appropriate data.*

a relation between said operations and data necessary for executing said operations; *The operation defined by the opcode defines a relation between the operation and the data upon which it will be performed.*

and a relation between said operations and data generated by said operations. *The operation defined by the opcode defines a relation between the operation and the data upon which it will be performed.*

28. As per claim 9, Mohamed teaches the program according to claim 6, wherein in order to start an operation or operations defined by said instruction or said instructions, an antecedent instruction which must have been executed is described. (Col. 1 lines 20-55)

Conclusion

29. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dillon Cody whose telephone number is 571-272-8401. The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJC

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